Drake, et al.; **U.S. Patent No.** 5,958,039 for "MASTER-SLAVE LATCHES AND POST INCREMENT/DECREMENT OPERATION" by Allen, et al.; and **U.S. Patent No.** 5,987,583 for "PROCESSOR ARCHITECTURE SCHEME AND INSTRUCTION SET FOR MAXIMIZING AVAILABLE OPCODES AND ADDRESSING SELECTION MODES" by Triece, et al. which are hereby incorporated herein by reference for all purposes.

In the Claims

Please cancel Claims 1 and 11, and amend the remaining claims as indicated below.

Applicants respectfully submit that no amendments have been made to the pending claims for the purpose of overcoming any prior art rejections that may restrict the literal scope of the claims or equivalents thereof.